REVIEW OF MICRO- AND NANOPROBE METROLOGY FOR DIRECT ELECTRICAL MEASUREMENTS ON PRODUCT WAFERS

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ABSTRACT

At the nanoscale, the electrical resistivity of solids is strongly and nonlinearly affected by their chemistry, crystallography, and geometry (e.g., critical dimensions). To achieve on-spec performance of semiconductor devices, an exceptional process control is thus essential. Four-terminal sensing is a well-established electric metrology, where resistivity is obtained from applying a known current across one pair of electrodes in contact with the sample, while measuring the voltage drop across another. Thanks to microfabrication, the downscaled Micro Four-Point Probes (M4PP) are characterized by (sub-)µm inter-electrode spacing, which enables to accurately determine resistivity on comparable length scales, while reducing the risk of current leakage through adjacent layers/devices. In addition to electrical resistivity (typically determined at a <0.1% precision), other key transport parameters can often be concurrently quantified (e.g., Hall carrier density and mobility, the temperature coefficient of resistance, and certain thermoelectric parameters). Here, we review milestones in M4PP development, showcase its characteristic use for in-line process monitoring of product wafers, and flag recent methodological improvements and advances.

IN-SITU FOUR TERMINAL SENSING ON THE MICROSCALE

Four-terminal measurements based on the van der Pauw theorem [1] are widely used in the semiconductor industry to monitor the deposition and annealing processes of metal and semiconductor thin films on the blanket wafer level. However, with a typical pitch of ~1 mm, and a contact force of ~1 N per electrode, most macroscopic four-point probes [e.g., 2] are rarely suitable for measurements on product wafers due to their large footprint, and the ensuing surface damage to the sample. In comparison, M4PPs have a typical pitch of 8 µm, and contact force of ~10 µN per electrode. When such probes are landed obliquely (at 30° to the probed surface), they exert minimal impact (if at all) on the probed surface, making M4PPs suitable for landing on metrology test pads located in scribe lines of product wafers. Another benefit of M4PP miniature size and gentle landing is that it reduces the risk of current leakage in thin multilayer samples through conductive layers below the layer of interest [3]. Key milestones in the miniaturization and automation of four-point probing at the microscale by CAPRES include:

a) the original straight cantilever design [4] (Fig. 1a),
b) vibration-tolerant L-shaped cantilevers [5] (Fig. 1b),
c) integrated surface detection (Fig. 1b-d) and automated probe change [6],
d) multi-cantilever (Figs. 1b-c) and non-equidistant (Fig. 1c) probes [7] down to sub-µm pitch [8], utilizing multi-electrode probing algorithms that eliminate geometric uncertainties [8-10], and
e) custom probe designs enabling the nondestructive probing of particularly fragile 3D nanostructures such as fins (Fig. 1d).

Current mainstream M4PP applications include the process control of ultra-shallow junctions [11], and in-line production monitoring of Magnetic Random-Access Memory (MRAM) devices [12].

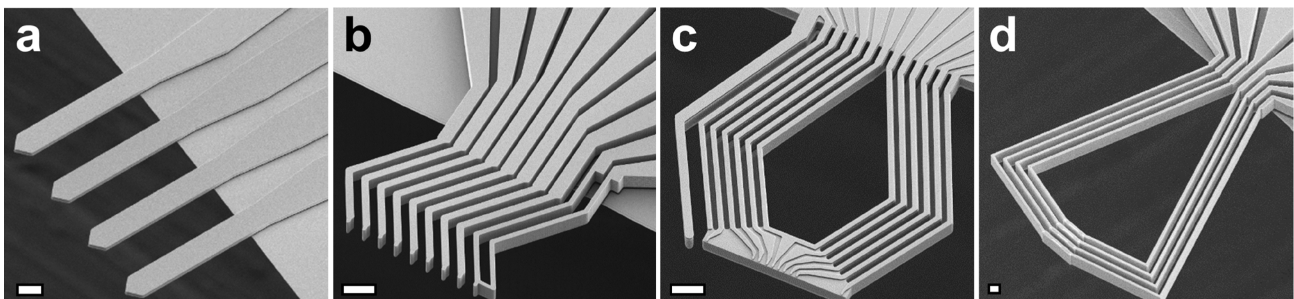

Figure 1: Evolution of CAPRES M4PPs during 2000–2020 (SEM images of the probes' contact surface facing up; bars are ~5 µm each): (a) the original, straight-cantilever, four-point probe design, (b) multi-cantilever, vibration-tolerant design, featuring a strain gauge for surface detection (the rightmost loop cantilever), (c) extreme small-pitch, non-equidistant, multi-cantilever probe (notice electrodes on top of a common, electrically-isolated, supporting plate), and (d) loop probe, for perpendicular engage on fragile elongated arrays of interconnects or fins.

SHEET RESISTANCE AND HALL CARRIER DENSITY AND MOBILITY

By applying a magnetic flux density normal to the surface of a conducting thin film, M4PP can be used to determine three key electromagnetic parameters of the thin film [13], namely:

a) Sheet resistance, R_{sq},
b) Hall sheet carrier density, N_{HS}, and
c) Hall carrier mobility, μ_H.

In the seminal study, the isolation of the magnetoresistive component required measurements at multiple locations approaching a straight boundary to a nonconductive medium [13]. Later, the measurement time was dramatically reduced via a multi-cantilever sampling at a single landing point in the vicinity (a few μm) of the half-plane boundary [9–10]. Most recently, and by utilizing the conformal mapping technique, accurate Hall effect measurements were demonstrated on rectangular pads of arbitrary dimensions, some as small as 70×70 μm^2 [14]; the latter technique has been accordingly termed by CAPRES as the Micro Hall Effect (MHE).

Here, we present the next generation of the CAPRES Micro Hall Effect module (MHE2; red symbols in Fig. 2a-c), which significantly improves on the original methodology (MHE; blue symbols in Fig. 2a-c) both in terms of better reproducibility (Fig. 2a), as well as reduced test pad dimensions (Fig. 2b). The first aspect of MHE2 has to do with a new design of experiment and of the data regression algorithm, which adopts the multi-cantilever geometric correction developed for M4PP Current-In-Plane Tunneling measurements [8]. Fig. 2a shows 25-point repeatability measurements performed using the L7PP probe [9] on a 25 nm thick $Si_{0.6}Ge_{0.4}$ thin film, benchmarking MHE against its successor MHE2. Both approaches yield matching (within their respective uncertainties) estimates of the sheet resistance (116.54 Ω/□), Hall sheet carrier density (3.32×10^{15} cm^{-2}) and Hall carrier mobility (16.15 cm V^{-1} s^{-1}), whilst the relative standard errors of the updated algorithm (MHE2) are two to five times lower, close or below the 0.1% limit.

The second improvement is due to a redesigned and twice as small probe (Fig. 1b), that can obtain reproducible measurements on significantly smaller test pads. Fig. 2b

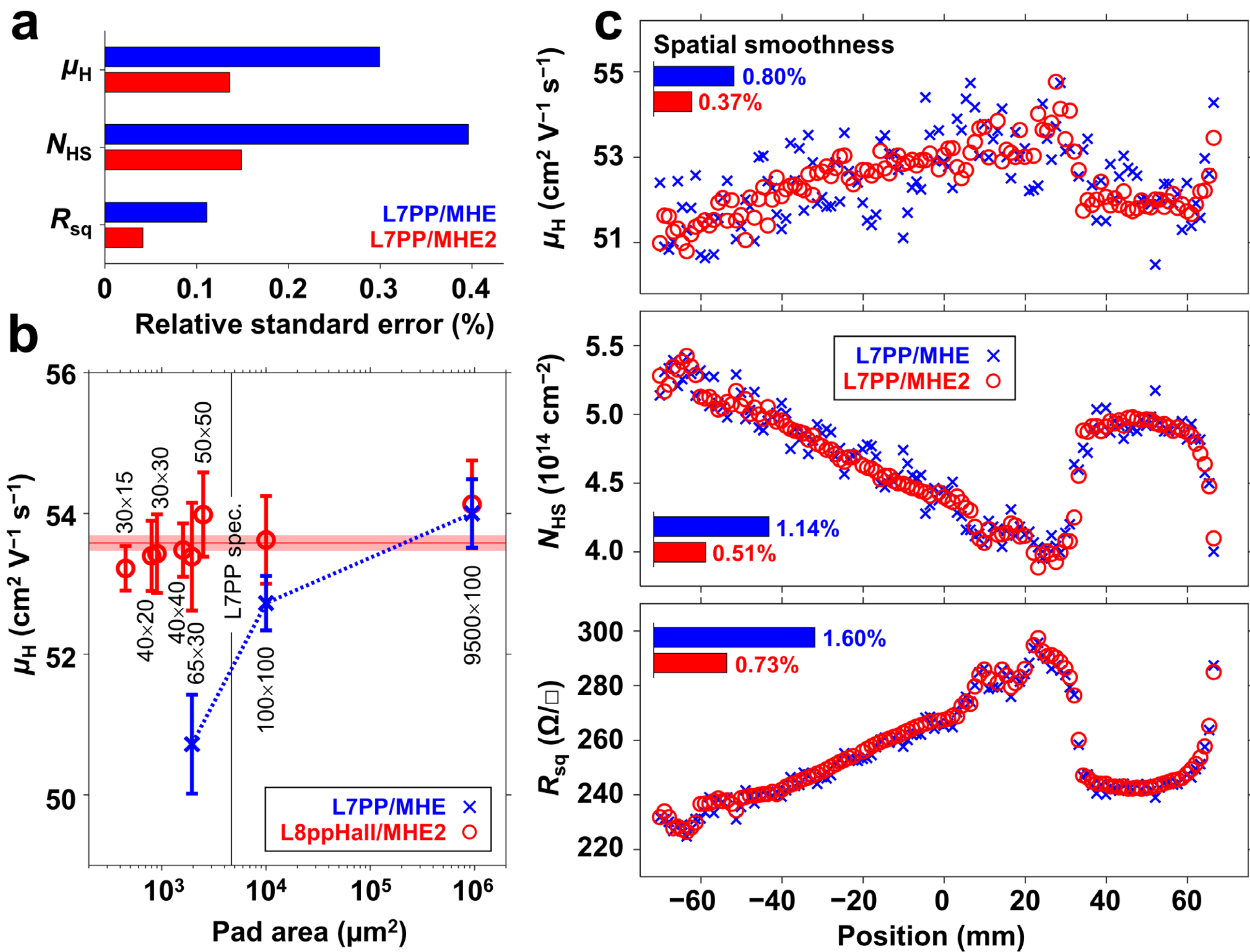

Figure 2: Next generation M4PP Micro Hall Effect measurements (MHE2), compared with its predecessor (MHE): (a) a two- to fivefold increase in reproducibility (N=25) via algorithm improvement, (b) elimination of pad size dependence, alongside a tenfold reduction in measurable pad size (pad dimensions in μm^2), and (c) a 150 mm patterned wafer transect, showing a twofold increase in spatial smoothness (reduction of unaccounted spatial variance).

compares Micro Hall Effect measurements (N=5 for each data point; error bars correspond to 1 standard error) of rectangular pads (ranging from 30×15 to 9450×100 μm^2 in size) of a patterned Boron-doped Si wafer ($B(11)^+$ implanted at 2 keV to 10^{15} cm^{-2}; annealed at 1100 °C for 30 s). One subset of the measurements (crosses in Fig. 2b) was carried out using the larger L7PP probe [9] and analyzed using the old MHE algorithm; the other subset (circles in Fig. 2b) was collected using the new L8ppHall probe (Fig. 1b) and analyzed via MHE2. In combination, the new probe and algorithm (L8ppHall/MHE2) demonstrate reproducible measurements and narrow uncertainties over 4 orders of magnitude of test pad area, exhibiting no pad size dependence (as does the L7PP/MHE combination beyond the probe's spec limits, cf. vertical line in Fig. 2b), and enabling accurate measurements of ca. tenfold smaller structures than previously possible.

To give an idea how Micro Hall Effect measurements on ~200−300 μm^2 test pads located in the scribe lines of a product wafer, could be used for in-line process control, Fig. 2c shows a line scan of sheet resistance and Micro Hall Effect measurements along the diameter of a 150 mm wafer (same sample as in Fig. 2b). The algorithm performance (MHE vs. MHE2) is evaluated through spatial smoothness, which we arbitrarily define here as the median of the relative differences across all pairs of neighboring sites (N=125 sites spaced 1 mm apart), i.e. median $[2|y_i - y_{i+1}|/(y_i + y_{i+1})]$, $i \in \{1, \ldots, N-1\}$. The MHE2 algorithm is not only visually smoother but yields a quantitative improvement by a factor of ~2.2 in all the regressed parameters (inset bar charts in Fig. 2c). Together with better reproducibility (Fig. 2a), we believe that this adds up to an order-of-magnitude increase in the method's spatial sensitivity (spatial resolving power), thus opening up new opportunities for in-line monitoring of process inhomogeneities on a tenfold finer scale than previously attainable.

CRITICAL DIMENSIONS, THERMAL EFFECTS, AND COMPLEMENTING CONTACTLESS THZ METROLOGY

Four recent M4PP applications (Fig. 3a-d), which extend the familiar domain of four-point electrical metrology, include:

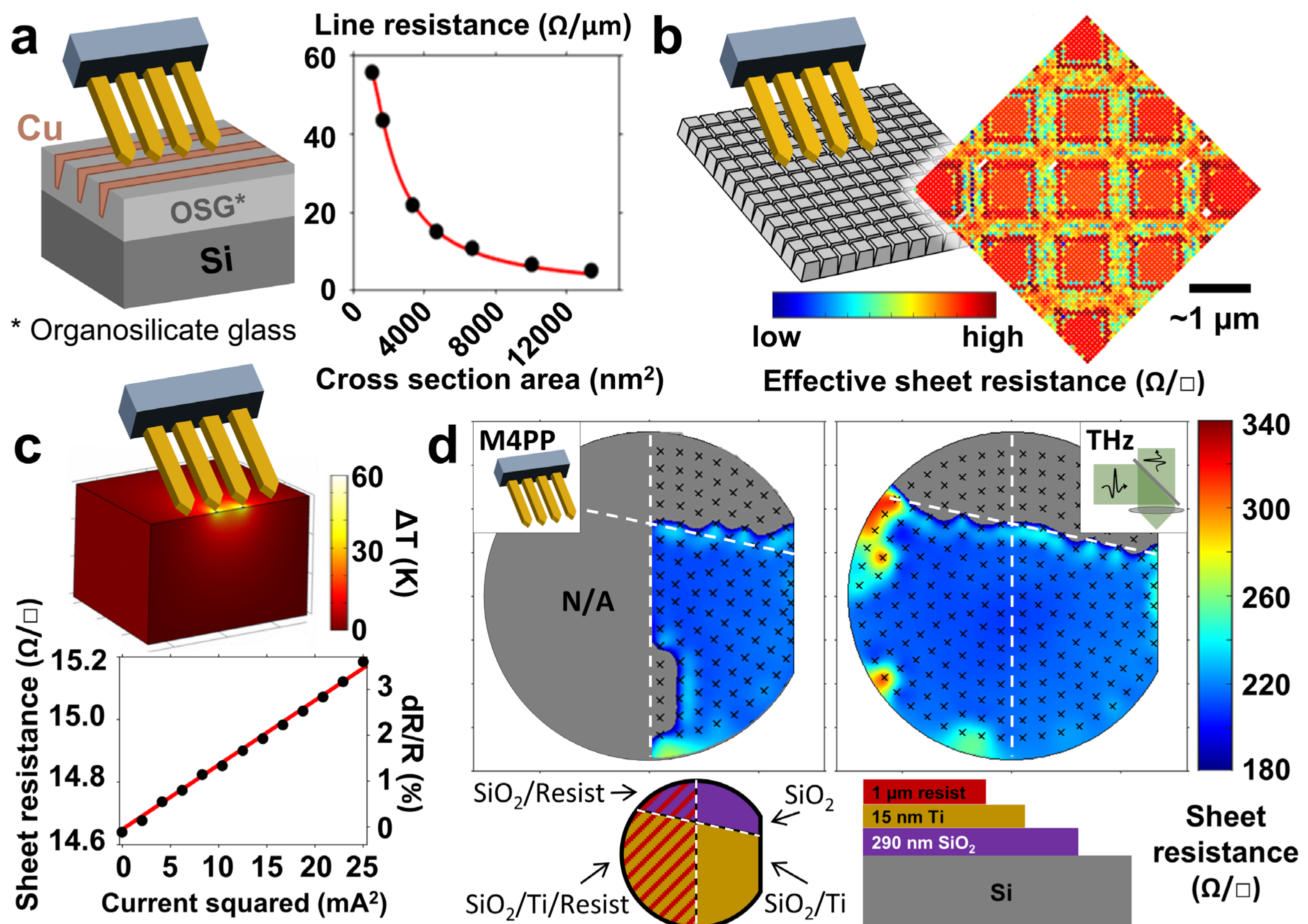

Figure 3: Recent CAPRES M4PP applications to measure on (a) nanowires, (b) doubly-periodic USJ, (c) TCR, and (d) buried metal layers (left: M4PP reference on exposed metal only; right: non-contact terahertz metrology seamlessly probing both exposed and buried metal; bottom: a color-matching top-view and cross-section of the wafer).

a) Non-destructive characterization of line resistance of nanoscale interconnects (Fig. 3a) as small as ~1000 nm^2 in cross section (~16 nm width). Small pads (50×50 µm) of tightly pitched interconnects, placed in the scribe lines of product wafers, can be used for performing in-line quality control measurements immediately after each successive metallization layer for process review and control, ultimately eliminating the need for monitor wafers.

b) Sheet resistance metrology of doubly-periodic square nanocomposites whose constituents have contrasting resistivities [15] can be achieved via small-area (e.g. ~6×6 µm in Fig. 3b) and densely-sampled (e.g. 100 nm steps in Fig. 3b) maps. These maps resolve the sub-µm spatial variation in resistance of 3D-patterned ultra-shallow junctions (USJ), which can be useful in cases where the resistivity gradient across cells and trenches is critical for device operation.

c) At sufficiently high sampling currents (~ mA range), M4PP exerts a considerable degree of Joule heating, which can be quantified to determine the Temperature Coefficient of Resistance (TCR) (Fig. 3c) [16]. During electrical probing, heating is localized to the M4PP volume and thus avoids the need to heat large areas, or to microfabricate and intercalibrate microheaters and thermocouples. Using a 3ω technique, the TCR contribution to resistance (the so-called "self-heating") can be corrected for [17], yielding more accurate (up to a percent level) estimates of the electromagnetic properties. The sensing of thermoelectric properties through the 2ω technique is currently under development [18].

d) To provide an alternative metrology for situations where no Ohmic contact can be established between the material or device of interest and the M4PP, CAPRES has recently integrated a non-contact electrical metrology module on its A301 tool, based on terahertz (THz) spectroscopy [19]. Such THz metrology is capable of sensing electrical characteristics (e.g., resistivity and carrier mobility) of buried conductive layers where traditional M4PP may fail (Fig. 3d) and is also capable of extracting carrier mobility from unpatterned films.

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Advanced metrology techniques for MRAM production monitoring

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Abstract

In recent years, embedded Spin Transfer Torque Magnetoresistive Random Access Memories (STT-MRAM) has been under intense development by leading semiconductor companies in terms of its integration and manufacturability in connection with standard CMOS microfabrication processes. By combining CIPT, MOKE and FMR metrologies, precise and accurate control, to monitor the magnetic and electrical properties of the STT-MRAM structures, is established in the backend of line, to avoid process excursions that can be costly and detrimental in terms of final product reliability.

Keywords—MRAM; MTJ; CIPT; microprobe; tunneling barrier; magnetic tunneling junction; MTJ; MOKE; FMR

Introduction

Embedded STT-MRAM is considered by far the most promising Non-Volatile Memory (NVM) solution for replacing embedded Flash memory, thanks to the reduced number of lithographic steps needed to produce embedded STT-MRAM arrays [1]. Moreover, thanks to the high read/write speed, high endurance and non-volatility, MRAM is also considered to become a low level cache memory, to be used in edge computing devices and automotive sensors and possibly as a storage class memory [1][2].

The core structure used within a STT-MRAM device is a Magnetic Tunneling Junction (MTJ), which is composed by a thin tunneling barrier of MgO sandwiched between ferromagnetic layers [2]. Among the many layers that constitute a MTJ junction, the key layers are the pinned layer and the storage layer, located right next to MgO barrier on opposite sites. By controlling the relative orientation of the magnetization between these two layers the electrical resistance, experienced by an electron current through the MgO barrier, can be controlled. Monitoring the electrical and magnetic properties of the MTJ right after the sputtering deposition of this complex multilayer structure and after the patterning of the MTJ layers into nanopillars, is of fundamental importance to achieve a high production yield as well as reliable final STT-MRAM based products (see Figure 2).

Wafer level CIPT, MOKE and FMR KLA metrologies

A. CIPT metrology

Current in plane tunneling (CIPT) metrology allows to measure the Resistance Area product in the parallel MTJ state (RA) and the Magnetoresistance (MR) by placing a microprobe in contact with the MTJ top surface and collecting a series of 4pp resistance values at different electrode spacings. In order to determine RA and MR the microprobes used for such measurement needs to have spacings between the electrodes that are close to the transfer length of the MTJ samples, which is typically in the range 0.15 μm to 1 μm [3] [4] (see Figure 1). This means that MEMS microprobes with electrode spacings down to 500 nm and electrode width of 250 nm need to be used. The uniformity of the RA across the 300 mm wafer area has a direct impact on the final nanopillar array electrical resistance distribution between devices and within the same array. CIPT metrology can also be used to determine the coercivity of the free layer (H_c) as well as the shift from zero field (H_{shift}). MR is linked to the final device read error rate given that determines the relative nanopillar resistance difference between the "zero" and "one" states, therefore it is relevant to monitor the MR variation across the wafer area (see Figure 2).

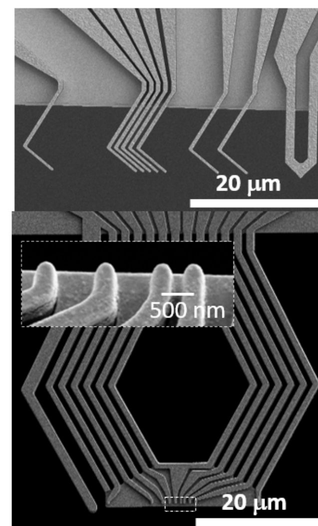

Figure 1. (Top) CIPT dedicated microprobe with minimum electrode spacing of 1.5 μm and a surface detector. (Bottom). CIPT dedicated Nanoloop probe with 10 electrodes and minimum spacing of 0.5 μm with integrated surface detector.

B. MOKE

Magneto-Optic Kerr Effect (MOKE) based metrology allows to map the hysteresis loop of the entire MTJ stack, including the pinned layer and the SAF layers across the wafer surface thanks to a 2.1 T electromagnet. From the hysteresis

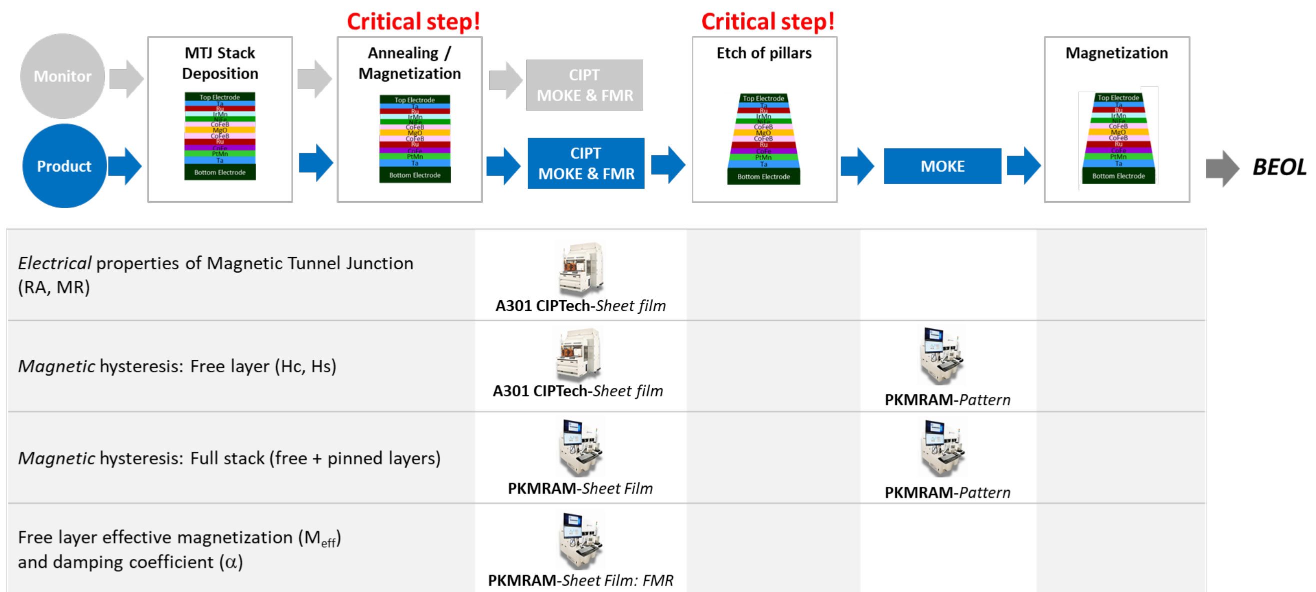

Figure. 2. KLA value proposition for STT-MRAM manufacturing control. The critical steps in the creation of the STT-MRAM devices are: 1) the PVD deposition of 10+ ultrathin layers of ferromagnetic and non-ferromagnetic materials, and the subsequent annealing, 2) The etching of the MTJ film into nanopillars to create the single memory cells. Measuring right after annealing, but before any further processing allows to establish the pristine electrical and magnetic properties of the MTJ before any degradation/shift is induced by the patterning or the thermal budget experienced by the MTJ pillars in the BEOL. Importantly, monitor wafers are only an indirect representation of the product MTJ stack given that they need to have modified bottom and top electrodes. Therefore, measuring on product wafers is the recommended solution to achieve a high yield.

loop it is possible to determine the coercivity fields and shifts for the free and pinned layers, as well as to verify the bistable behavior of the MTJ stack [4]. Importantly, MOKE metrology can be used to verify the magnetic properties of the nanopillars after the patterning of the MTJ stack into memory cells and before any further metallization is completed (see Figure 2). The optimization of the etching of the MTJ stack has been, and still is, one of the key challenges in the fabrication of STT-MRAM devices, due to the presence of residue on the sidewalls of the pillars as well as degradation of the magnetic properties after shaping the MTJ stack in nanopillars of dimension between 30-100 nm in diameter [5].

C. FMR

Ferro Magnetic Resonance (FMR) based metrology allows the non-contact measurement of absolute free layer effective magnetization, the damping coefficient, and the inhomogeneous loop broadening. These parameters are linked to the final switching current of the single cell device [6][7]. FMR metrology technique has now been extended to allow the mapping of these parameters over the full 300 mm wafer surface.

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